

High-speed reverse converter (HISPREC) for improving reliability in wireless sensor networks

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Abstract: Wireless Sensor Networks (WSNs) consist of huge quantities of sensor hubs that are distributed in an unfriendly environment which are used to monitor the environment and check physical conditions. It has been proven that vitality, speed and reliability are the most obliging components on the functionality of WSNs as they are controlled with constrained vitality and limited hardware resources. Thus, WSN must be designed in an energy-efficient and reliable manner. However, the intrinsic properties of carry-free operations, parallelism and adaptation to internal failure of Residue Number System (RNS) have made it a promising strategy for high-speed arithmetic and low power utilisation for WSN applications. Hence, to reduce power utilisation and improve message reliability in WSNs, High Speed REverse Converter (HISPREC) is proposed in this article. The paper is aimed at designing high speed and low vitality utilisation reverse converter to improve the reliability and diminish conversion delay in real-time WSNs. The proposed reverse converter (HISPREC) is designed for the moduli set $\{2^{n+1}-1, 2^n, 2^n-1\}$ and actualised using Mixed Radix Conversion (MRC). The results of theoretical and experimental simulations show that HISPREC outstripped existing reverse converters as far as speed, hardware requirements, vitality utilisation and conversion delay all of which affect the reliability of the received information in real-time WSNs.

Keywords: Wireless sensor network; energy consumption; reliability; reverse converter; residue number system

1. Introduction

Wireless Sensor Networks (WSNs) are evolving technology that consist of enormous amount of minute low-cost vitality inadequate nodes which have small capabilities of identifying, processing and transmitting message through radio transceiver (Demigha et al., 2011; Jindal, 2018). They are wireless networks comprising of spatially disseminated independent devices utilising sensors to observe physical conditions or environmental situations such as temperature, sound, pressure, and cooperatively pass their sensed data through the network to the sink which delivers wireless connectivity back to the end users (Khodabande et al., 2013; Barati et al., 2014). Hence, WSNs have prospective of considerably

improving the capacity to observe and cooperate with physical environment (Roshanzadeh & Saqaeean, 2012). In WSNs applications, vitality utilisation is the major challenge because the sensor hubs have inadequate source of power which is difficult to replace or even revitalise after distribution (Demigha et al., 2011; Barati et al., 2014; Lee et al., 2016). Hence, WSNs need to be planned in an energy-efficient manner. Similarly, data aggregation is another major challenge affecting speed and reliability of WSNs, thus, there is need to eliminate data aggregation during message transmitting. Usually, WSNs are used to collect vital information from the environment and are required to send reliably sensed message speedily. Thus, to maintain message reliability, it is required to provide satisfactory mechanisms for

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sensor hubs to send correct sensed data quickly and the sink to convert the received message accurately and at high speed.

Various techniques could be used to reduce power consumption and provide high speed operations in order to improve reliability in real-time WSNs. Low Energy Adaptive Clustering Hierarchy (LEACH) algorithm is the first and most effective energy-efficient hierarchical clustering algorithm for WSNs that was proposed for reducing power consumption (Hamamreh et al., 2018). But message aggregation in LEACH usually causes delay in sending received packets from the CH to the sink. However, Residue Number System (RNS) has also been utilised as a mechanism to lessen transmission vitality and increase unwavering quality in WSNs. RNS is a non-weighted number system that could be utilised for energy-efficient and reliable WSN operations because it offers carry-free, parallel, high-speed, secure, and fault tolerant arithmetic operations. RNS can thus be incorporated to LEACH to eliminate data aggregation and improve network reliability because it offers unlimited potential for high-speed computer arithmetic (Gbolagade & Cotozana, 2009; Abdul-Mumin & Gbolagade, 2016).

However, to improve message reliability in WSNs, High Speed REverse Converter (HISPREC) is proposed in this article. HISPREC is designed using RNS for the moduli set $\{2^{n+1}-1, 2^n, 2^n-1\}$ and implemented based on MRC to reduce vitality utilisation, hardware requirements, congestion and provide high speed operations in WSNs. In HISPREC, the sensor nodes transmit the residues of the sensed data instead of the original message, therefore fewer packets are sent, vitality consumption is reduced, transmission speed is increased, and reliability is improved. Then, a reverse converter is used to decode the received packets to recover the original message. The simulation results show that HISPREC outperforms existing reverse converter in terms of vitality utilisation, speed, hardware requirements and delay in converting the residues all of which have direct effect on the reliability of the sensor network.

2. Literature review

Several researches have been carried out to explore diverse areas in vitality utilisation and speed for reliable WSNs. Those researches have brought new tasks in providing high speed, secured and reliable message identifying and communication in WSNs. However, Ye et al. (2018) examined a REliable reSIDuE number system-based data transmission mechanism (RESIDENT) for WSNs to enhance data communication

consistency through hybrid automatic repeat requests (ARQ) in hop-by-hop situations. A novel decode scheme was designed to reduce the algorithm complexity and then combined ARQ to enhance data communication consistency. However, the transmission technique is appropriate for high packet reception rate and low packet reception rate scenarios. The simulation results indicated that RESIDENT enhances communication reliability in terms of amount of packet received and end-to-end delay but with less vitality utilisation in low packet reception rate scenario. Correspondingly, Barati et al. (2014) proposed a novel energy conservation and high speed error control with an efficient reverse converter using MRC for the moduli set $\{2^{2n+1}, 2^{2n+1}-1, 2^{n-1}\}$ and accomplished substantial enhancements both in terms of vitality proficient and conversion delay but with little hardware requirements. Nevertheless, the moduli set is a fixed set and cannot be adjusted to the rate of redundancy according to the demands of a real-world scenario.

Also, Hamamreh et al. (2018) present a new energy-aware algorithm named Minimum Residual Hop Capacity (MRHC). The algorithm was incorporated into the most commonly used protocol called Low Energy Adaptive Cluster Hierarchical (LEACH) in the transmission process within clusters. This reduced energy utilisation in the transmission process, extend network lifetime and improved the amount of data delivered to the base station. Usually, nodes communicate within cluster through multi-hop communications and data is sent through other nodes in the cluster until it reaches the CH. This result in few duplicates of a similar packet could get to the CH, hence there is need for data aggregation which usually causes communication delay between the CH and the sink. Furthermore, Han et al., (2015) examined approximation algorithms with incontestable performance ratios based on a new data architecture called Time-Reliability-Power space. The model takes into account several aspects comprising duty cycling, wireless broadcast advantage, unreliable links, and power adjustability, as well as providing guaranteed performance bounds for energy-efficient reliable data dissemination in duty cycle WSNs. Simulation results demonstrated the practical efficiency of the algorithms when compared with other state of the art algorithms. However, duty cycle approach always results in an expanded hub multifaceted nature and system idleness. Finally, Mohammad et al. (2017) proposed Syncast, a protocol to improve synchronous transmission by exploiting capture effect over multichannel. The evaluation shows that Syncast provides a robust,

reliable, and scalable data dissemination of large packets with lower end-to-end delay and up to 92% reduced radio-on-time. It is observed that since no single approach has provided energy efficient and extensive reliability support for WSN. Hence, it is essential to develop an improved reverse converter that would enhance the conversion speed with minimal hardware requirements and reduced power utilisation to improve reliability in WSNs.

3. Materials and methods

In the HISPREC, the sensor nodes are divided into clusters and sensor node with higher resources is selected as the cluster head (CH). The CH organises all the activities within its cluster. It is also the responsibility of the CH to gather information from cluster nodes and send to another CH until the message reaches the base station.

Each sensor node uses the moduli set to split the sensed data into some smaller packets which are independent and operations can be accomplished on them separately and concurrently. The residues of the sensed message with respect to the moduli set are transmitted instead of the sensed message itself. Hence, fewer packets are sent and this would make the computations simpler, much faster, and with reduced power consumption. However, the sensor nodes would send a residue of the sensed data based on its Id in the cluster to the cluster head (CH), this has eliminated the need for data aggregation. Then, CH would collect all the residues from all the nodes in the cluster and send to another CH or the sink. The sink knowing that the CH in the network would transmit the residues, instead of the original message would require a reverse converter to decode the received packets in order to recover the original message as shown in Figure 1.

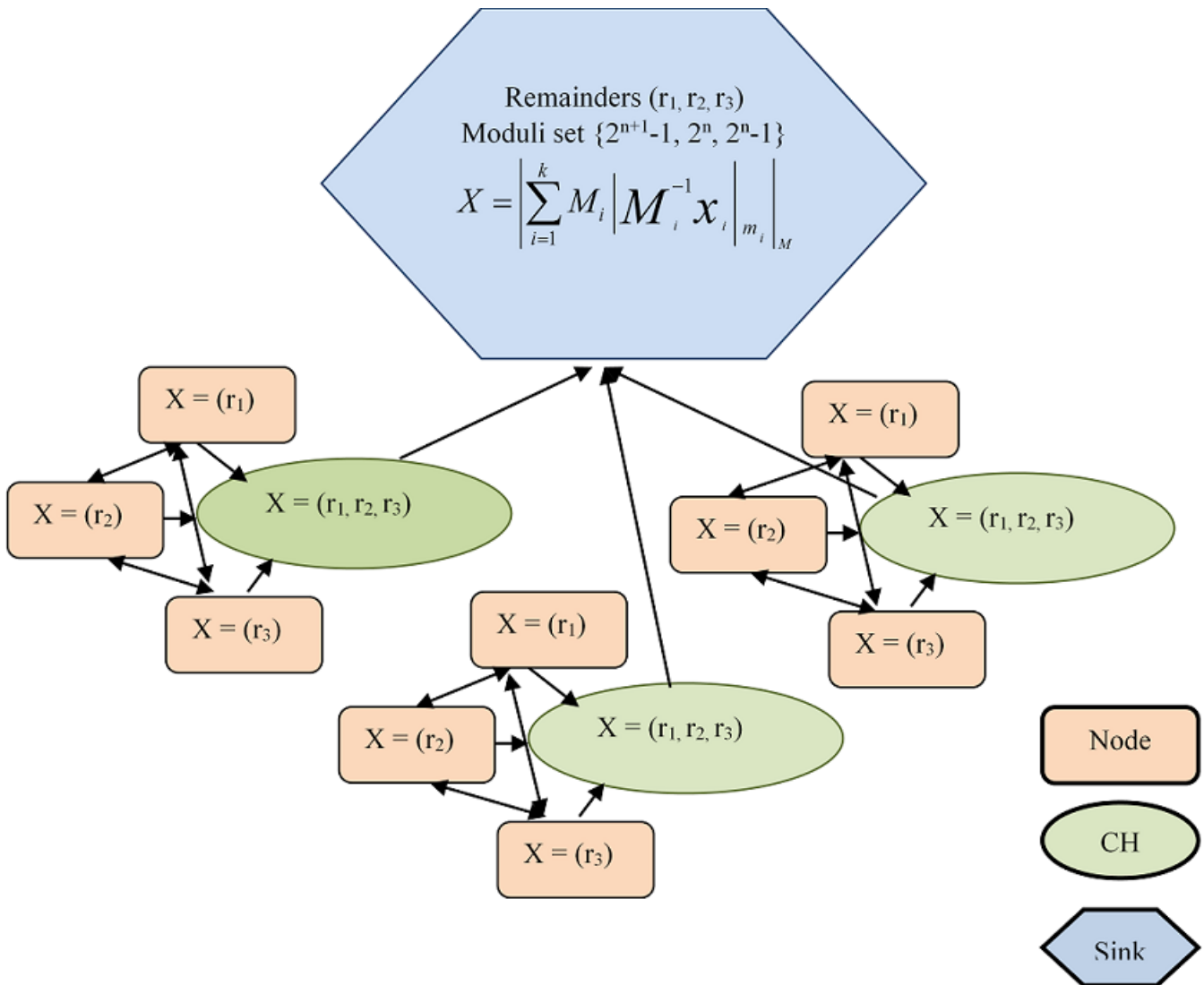


Figure 1: Message transmission in HISPREC

3.1. Design of the reverse converter

The design of the proposed HISPREC for improving reliability in real-time WSNs is presented in this subsection. Consider RNS which is based on the congruence relation is described in terms of relatively prime moduli set $\{m_1, m_2, \dots, m_n\}$ and that the greatest common divisor $\gcd(m_i, m_j) = 1$ for $(i \neq j)$. Thus, a weighted number X can be represented as

$$X = (x_1, x_2, \dots, x_n), \text{ where:} \\ x_i = x \bmod p_i = \lfloor x \rfloor p_i, 0 \leq x_i < p_i \quad (1)$$

It is worth noting that such a representation is unique for any integer X in the range $[0, M)$ where $M = (m_1 X m_2 X \dots X m_n)$ is referred to as dynamic range of the moduli set $\{m_1, m_2, \dots, m_n\}$. In addition, Chinese Remainder Theorem (CRT) and Mixed Radix Conversion (MRC) are the two basic approaches for an efficient reverse converter to convert from RNS to its binary equivalent. MRC is selected because of its reliability in data delivery, required hardware, vitality utilisation and network delay are reduced which in turn increase reliability (Omondi & Premkumar, 2007; Barati et al., 2014). The moduli set was proposed to streamline the implementation of hardware and arithmetic operations of HISPREC.

Therefore HISPREC can easily be derived using MRC algorithm as follows:

$$X = a_1 + a_2 m_1 + a_3 m_1 m_2 + \dots + a_n m_1 m_2 m_3 \dots m_{n-1} \quad (2)$$

And the coefficients a_i can be obtained from residue by

$$a_1 = x_1 \quad (3)$$

$$a_2 = \left| (x_2 - a_1) \right|_{m_1}^{-1} \Big|_{m_2} \quad (4)$$

$$a_3 = \left| ((x_3 - a_1) \right|_{m_1}^{-1} \Big|_{m_3} - a_2 \right|_{m_2}^{-1} \Big|_{m_3} \quad (5)$$

...

...

Therefore, a_n is generally given as:

$$a_n = \left| (((x_n - a_1) \right|_{m_1}^{-1} \Big|_{m_n} - a_2) \right|_{m_2}^{-1} \Big|_{m_n} - \dots - a_{n-1} \Big|_{m_{n-1}}^{-1} \Big|_{m_n} \quad (6)$$

Where $\left| m_i - 1 \right|_{mn}$ denotes multiplicative inverse of m_i with respect to m_j . However, it important to mention that multiplicative inverse for a number X is a number

that when multiplied by X yields the multiplicative identity of 1. The extended Euclidean algorithm can be used to derive modular multiplicative inverse of a modulo m .

Furthermore, HISPREC can be designed for the moduli set $\{2^{n+1}-1, 2^n, 2^n-1\}$ with three corresponding residues (x_1, x_2, x_3) . However, in order to design the converter, there is need to demonstrate that the moduli set $\{2^{n+1}-1, 2^n, 2^n-1\}$ are pair wise relative prime. This can be achieved using Euclidean algorithm:

$$\gcd(a, b) = \gcd(b, \lfloor a \rfloor b), \quad a > b \quad (7)$$

where $\gcd$ is the greatest common divisor, therefore:

$$\gcd(2^{n+1}-1, 2^n) = \gcd(2^n, \lfloor 2^{n+1}-1 \rfloor 2^n) = \gcd(2^n, 1) = 1 \quad (8)$$

$$\gcd(2^{n+1}-1, 2^n-1) = \gcd(2^n-1, \lfloor 2^{n+1}-1 \rfloor 2^n-1) = \gcd(2^n-1, 2) = 1 \quad (9)$$

$$\gcd(2^n, 2^n-1) = \gcd(2^n-1, \lfloor 2^n \rfloor 2^n-1) = \gcd(2^n-1, 1) = 1 \quad (10)$$

From the above proofs, it is obvious that all the proposed moduli set $\{2^{n+1}-1, 2^n, 2^n-1\}$ are relatively prime, because all the greatest common divisors ($\gcd$) are equal to 1.

Next is to compute the multiplicative inverse based on MRC algorithm and then replace these values with the modulus set in the conversion algorithm with the following prepositions.

Given the moduli set $\{2^{n+1}-1, 2^n, 2^n-1\}$ with $m_1 = 2^{n+1}-1$, $m_2 = 2^n$, and $m_3 = 2^n-1$ then the following preposition are true.

Proposition 1: The multiplicative inverse of $(2^{n+1}-1)$ with respect to (2^n) is $Y_1 = -1$

Proof: If it can be proved that $\left| m_1 Y_1 \right|_{m_2} = 1$, which simply means that -1 is the multiplicative inverse of m_1 with respect to m_2 .

$$\left| m_1^{-1} \right|_{m_2} = \left| (2^{n+1}-1)^{-1} \right|_{2^n} = \left| (-1 \times 2^{n+1}-1) \right|_{2^n} = 1 \quad (11)$$

$$\text{Therefore } \left| m_1^{-1} \right|_{m_2} = -1$$

Proposition 2: Also the multiplicative inverse of $(2^{n+1}-1)$ with respect to (2^n-1) is $Y_2 = 1$

Proof: If it can also be proved that $\left| m_1 Y_2 \right|_{m_3} = 1$, which simply means that 1 is the multiplicative inverse of m_1 with respect to m_3 .

$$|m_1^{-1}|_{m_3} = |(2^{n+1} - 1)^{-1}|_{2^n - 1} = |(1.2^{n+1} - 1)|_{2^n - 1} = 1 \quad (12)$$

$$\text{Therefore } |m_1^{-1}|_{m_3} = 1$$

Proposition 3: And lastly the multiplicative inverse of (2n) with respect to (2n-1) is $Y_3 = 1$

Proof: If it can also be proved that $|m_2 Y_3|_{m_3} = 1$, which simply means that 1 is the multiplicative inverse of m_2 with respect to m_3 .

$$|m_2^{-1}|_{m_3} = |(2^n)^{-1}|_{2^n - 1} = |(1.2^n)|_{2^n - 1} = 1 \quad (13)$$

$$\text{Therefore } | \quad | \quad 1$$

Then, since the values of $Y1 = -1$, $Y2 = 1$, $Y3 = 1$, $m1 = 2n + 1 - 1$, $m2 = 2n$ and $m3 = 2n - 1$. In equations (2) to (6) the MRC is given by:

$$X = a_1 + a_2 m_1 + a_3 m_1 m_2 \quad (14)$$

Where

$$a_1 = x_1 \quad (15)$$

$$a_2 = |(x_2 - a_1)|_{m_1^{-1}}|_{m_2}|_{m_3} \quad (16)$$

$$a_3 = |((x_3 - a_1)|_{m_1^{-1}}|_{m_3} - a_2)|_{m_2^{-1}}|_{m_3}|_{m_3} \quad (17)$$

The above equation (17) can be simplified to decrease the hardware complexity

$$\begin{aligned} a_2 &= |(-1)(x_2 - a_1)|_{m_2} \\ a_2 &= |-1(x_2 - a_1)|_{2^n} \\ a_2 &= |-x_2|_{2^n} + |a_1|_{2^n} \end{aligned} \quad (18)$$

And also equation (18) can be simplified to decrease the hardware requirements

$$\begin{aligned} a_3 &= |(1(x_3 - a_1) - a_2)(1)|_{m_3} \\ a_3 &= |(x_3 - a_1) - a_2|_{2^n - 1} \\ a_3 &= |x_3|_{2^n - 1} + |-a_1|_{2^n - 1} + |-a_2|_{2^n - 1} \end{aligned} \quad (19)$$

Then from equations (15, 18 and 19) we have

$$\left\{ \begin{aligned} X &= x_1 + |(-1)(x_2 - a_1)|_{m_2} (2^{n+1} - 1) \\ &+ |(1(x_3 - a_1) - a_2)(1)|_{m_3} (2^{n+1} - 1 \times 2^n) \end{aligned} \right\} \quad (20)$$

$$\left\{ \begin{aligned} X &= x_1 + |(-x_2 + a_1)|_{m_2} (2^{n+1} - 1) \\ &+ |(x_3 - a_1) - a_2|_{m_3} (2^{n+1} - 1 \times 2^n) \end{aligned} \right\} \quad (21)$$

$$\left\{ \begin{aligned} X &= x_1 + (|-x_2|_{2^n} + |a_1|_{2^n})(2^{n+1} - 1) \\ &+ (|x_3|_{2^n - 1} + |-a_1|_{2^n - 1} + |-a_2|_{2^n - 1})(2^{n+1} - 1 \times 2^n) \end{aligned} \right\} \quad (22)$$

$$\left\{ \begin{aligned} X &= x_1 + (2^{n+1} - 1) \times |-x_2|_{2^n} + |a_1|_{2^n} \\ &+ (2^{n+1} - 1 \times 2^n) \times |x_3|_{2^n - 1} + |-a_1|_{2^n - 1} + |-a_2|_{2^n - 1} \end{aligned} \right\} \quad (23)$$

Moreover, to design HISPREC, there is need to simplify equation (18) and (19) as follows:

$$\begin{aligned} a_2 &= |(x_2 - a_1)|_{m_1^{-1}}|_{m_2}|_{m_3} = |-x_2|_{2^n} + |a_1|_{2^n} \\ &= |-x_2|_{2^n} + |x_1|_{2^n} = a_{21} + a_{22} \end{aligned}$$

Therefore, the binary representation of the residues will be:

$$a_{21} = |-x_2|_{2^n} = \underbrace{\bar{x}_{2,n-1} \bar{x}_{2,n-2} \dots \bar{x}_{2,1} \bar{x}_{2,0}}_{nbit} \quad (24)$$

$$a_{22} = |x_1|_{2^n} = \underbrace{x_{1,n-1} x_{1,n-2} \dots x_{1,1} x_{1,0}}_{nbit} \quad (25)$$

3.2. Implementation of HISPREC

However, for the implementation of a_2 based on equations (24) and (25), (n) bits Carry Save Adder (CSA) with End Around Carry (EAC) and a (n) bits Carry Propagate Adder (CPA) with EAC. This is because there are three (n) bits input as shown in the implementation of a_2 as shown in Figure 2.

It is worth mentioning that for implementation of equation 24, there is need to have (n+1) NOT gates that are prepared using operand preparation unit (1) – OPU(1).

Next is to implement a_3 based on simplifying equation (19) as follows:

$$\begin{aligned} a_3 &= |(1(x_3 - a_1) - a_2)(1)|_{m_3} = |(x_3 - x_1) - a_2|_{2^n - 1} \\ &= |x_3|_{2^n - 1} + |-x_1|_{2^n - 1} + |-a_2|_{2^n - 1} = a_{31} + a_{32} + a_{33}, \end{aligned}$$

where the binary representation of the residues will be:

$$a_{31} = |x_3|_{2^n-1} = \underbrace{x_{3,n-1} x_{3,n-2} \dots x_{3,1} x_{3,0}}_{(n) \text{ bit}} \quad (26)$$

$$a_{32} = |-x_1|_{2^n-1} = \underbrace{\bar{x}_{1,n-1} \bar{x}_{1,n-2} \dots \bar{x}_{1,1} \bar{x}_{1,0}}_{(n) \text{ bit}} \quad (27)$$

$$a_{33} = |-a_2|_{2^n-1} = \underbrace{\bar{a}_{2,n-1} \bar{a}_{2,n-2} \dots \bar{a}_{2,1} \bar{a}_{2,0}}_{(n) \text{ bits}} \quad (28)$$

Also, there is need of (n) bits CSA with EAC and a (n) bits CPA with EAC to implement a_3 based on equations (26) to (28) as shown in Figure 3.

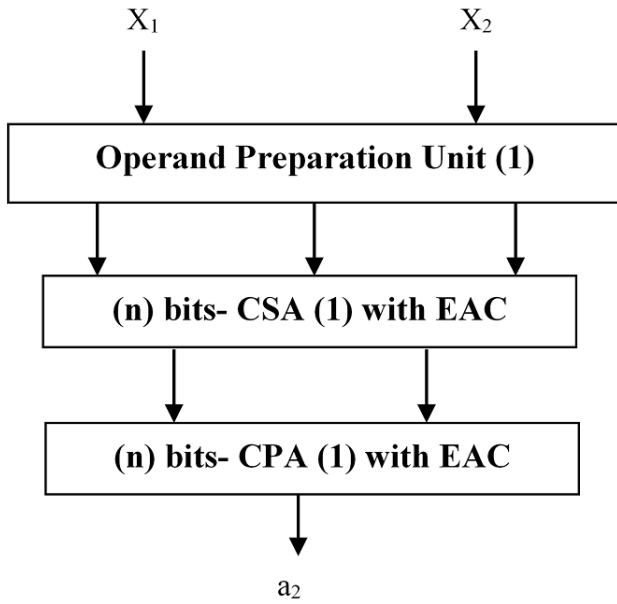


Figure 2: Implementation of a_2 based on equations 24 and 25

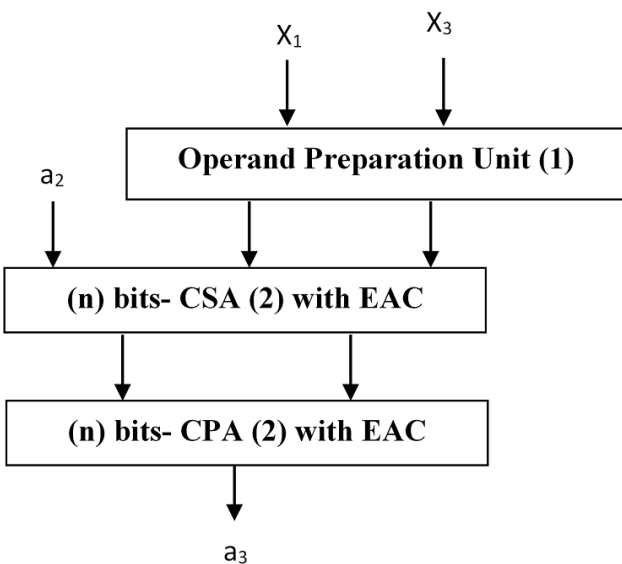


Figure 3: Implementation of a_3 based on equations 26 and 28

Lastly, we can now obtain X based on the equation (14), we have

$$\begin{aligned} X &= a_1 + a_2 m_1 + a_3 m_1 m_2 \\ &= x_1 + m_1 (a_2 + a_3 m_2) \end{aligned}$$

$$= x_1 + (2^{n+1} - 1) \underbrace{(a_2 + (2^n) a_3)}_C \quad (29)$$

$$= x_1 + (2^{n+1} - 1) C \quad (30)$$

$$C = a_2 + (2^n) a_3 \quad (31)$$

$$\left\{ C = \underbrace{a_{3,n-1} \dots a_{3,0}}_{(n-1) \text{ bits}} \underbrace{a_{2,n-1} a_{2,n-2} \dots a_{2,n}}_{1 \text{ bit}} \underbrace{\bar{a}_{3,n-1} \dots \bar{a}_{3,0}}_{(n) \text{ bits}} + \underbrace{1 \dots 1}_{(n) \text{ bits}} \underbrace{a_{2,n-1} \dots a_{2,0}}_{(n) \text{ bits}} \right\} \quad (32)$$

$$X = x_1 + (2^{n+1} - 1) C = \text{Concatenation of } (x_1, C)$$

$$\left\{ X = \underbrace{C_{3n} \dots C_n}_{(n+1) \text{ bits}} \underbrace{C_{n-1} \dots C_0}_{(n) \text{ bit}} \underbrace{\bar{C}_{n+1} \dots \bar{C}_0}_{(n+1) \text{ bits}} + \underbrace{1 \dots 1}_{(n+1) \text{ bits}} \underbrace{\bar{C}_{3n} \dots \bar{C}_{n+1}}_{(n) \text{ bits}} \times \underbrace{x_{1,n+1} \dots x_{1,0}}_{n+1} \right\} \quad (33)$$

Therefore, the implementation of X is given in Figure 4.

However, for implementation of X, consider equations 32 and 33, there is need for $(2n)$ bits and $(3n+2)$ bits Regular CPA. Also, there is need for OPU (2) and (3) for preparing the 1's complements in equations 32 and 33 respectively. However, (n) bits and $(n+1)$ bits are 1 in equations 31 and 32 respectively. Therefore (n) and $(n+1)$ full adders (FAs) can be replaced with (n) and $(n+1)$ pairs of OR/XNOR gates in equations 31 and 32 respectively. Table 1 displays area and delay requirements of the proposed reverse converter based on MRC for the moduli set $\{2^{n+1}-1, 2^n, 2^{n-1}\}$.

The area and delay specification for HISPREC in real-time WSN can be generated as follows:

$$\begin{aligned} \text{Total area} &= (6n+2)A_{FA} + (3n+2)A_{NOT} + (3n+1)A_{XNOR} \\ \text{Total delay} &= (9n+2)A_{FA} + 3t_{NOT} \end{aligned}$$

4. Performance evaluation

Performance evaluation of HISPREC was done by comparing it with the existing reverse converters. The results of theoretical analysis are presented in

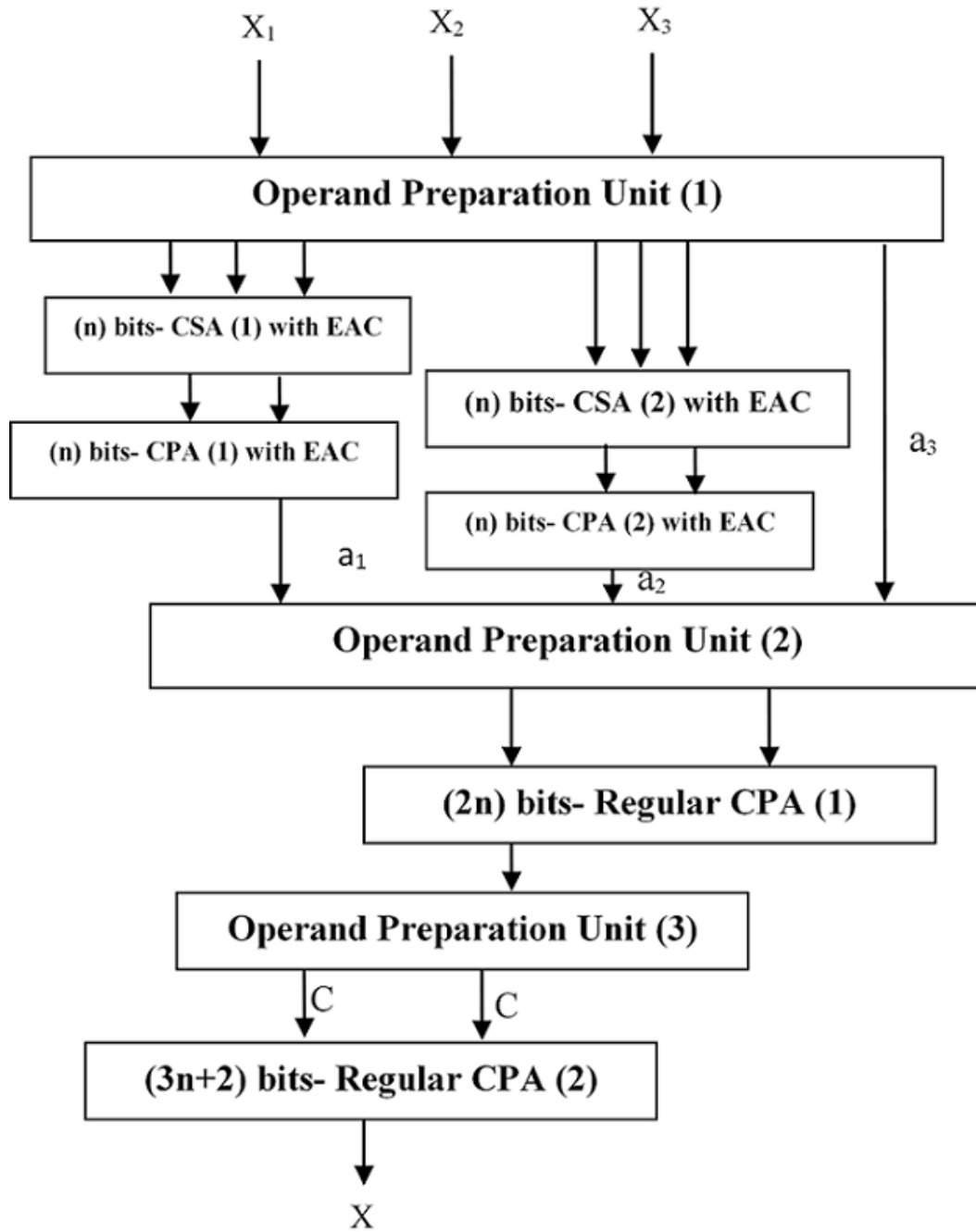


Figure 4: Implementation of X based on equations 32 and 33

Table 2. It is worth noting that for reverse converters with dissimilar dynamic range to be fairly evaluated, they should be evaluated under the same conditions and compete favourably. This table shows that in terms of area and delay HISPREC is efficient when compared with some existing reverse converter in terms of vitality utilisation, conversion speed, hardware requirements and reliability of the sent data.

Furthermore, Probabilistic wireless network simulator (Prowler) running under MATLAB was utilised to create the entire simple WSN system to illustrate the experimental simulation. MATLAB offers collaborating environment with many reliable and accurate built-in mathematical functions. Similarly, Prowler offers a stress-free way of application prototyping and ability to simulate wireless distributed systems. This Simulation

Table 1: Characterization of each part of HISPREC for the moduli set $\{2^{n+1}-1, 2^n, 2^n-1\}$

Parts	FA	NOT	OR/XNOR	Delay
OPU (1)	----	$(n+1)$	----	t_{NOT}
CSA (1)	1	----	n	t_{FA}
CPA (1)	n	----	----	$(2n)t_{FA}$
CSA (2)	n	----	----	t_{FA}
CPA (2)	n	----	----	$(2n) t_{FA}$
OPU (2)	----	n	----	t_{NOT}
R-CPA (1)	n	----	$(n+1)$	$(2n+1) t_{FA}$
OPU (3)	----	$(n+1)$	----	t_{NOT}
R-CPA (2)	$(2n+1)$	----	n	$(3n+1)t_{FA}$

Table 2: Area and delay comparison

Reverse Converter	Moduli Set	Area (A_{FA})	Delay (t_{FA})
Bankas and Gbolagade (2014)- BG[14]	$\{2^n, 2^n + 1, 2^n - 1, 2^{2n+1} - 1\}$	$12n+2$	$9n+6$
Barati, Movaghar and Sabaei (2014)- BMS[14]	$\{2^{2n+1}, 2^{2n+1}-1, 2^n-1\}$	$7n+3$	$9n+8$
Raju, Kumar and Divya (2014)- RKD[14]	$\{2^{n+1}, 2^n-1, 2^{2n}, 2^{2n+1}-1\}$	$10n+2$	$14n+3$
Habibi and Salehnamadi (2016) – HS[16]	$\{2^n-1, 2^{n+1}, 2^{2n}-1\}$	$5n + 1$	$10n + 6$
HISPREC	$\{2^{n+1}-1, 2^n, 2^n-1\}$	$6n + 2$	$9n + 2$

technique comprises assembling the hardware construction of the transmitting hubs, modeling both the communication channel and the receiving sink. Furthermore, the simulation model was examined by engaging different amounts of sensor hub, energy capability and topologies under various conditions. Several results were gathered from the performance evaluation of HISPREC with other reverse converters in terms of vitality utilisation, conversion speed, delay and hardware requirements. 100 nodes were randomly deployed over an area of 100 square meters, (i.e. the radio coverage of each sensor node and sink was assumed to be a circular area of 100m in diameter). Initial energy of each sensor nodes was set to 10 Joule of energy. All simulations were repeated 5 times for different set of n before computing the average of the results. Figure 5 indicates 100 sensor hubs that were consistently dispersed over a 150m×150m territory with different evaluation results for vitality consumption, hardware requirements and conversion delay as shown in Figures 6-8.

5. Results and discussion

Realisation of sensor networks needs to satisfy the factors such as fault tolerance, scalability, cost, hardware limitations, topology change, network dynamics, and power management. One of the important constraints is reliability support for various challenging issues of WSN. Since these constraints are highly stringent and specific for sensor networks, wireless sensor networks are required to provide different levels of reliability based on the type of applications. However, reliability may be affected by factors such as scalability, redundancy in data transmission, energy management, unbalanced traffic etc. The HISPREC for the moduli set $\{2^{n+1}-1, 2^n, 2^n-1\}$ has dynamic range of $3n + 1$ which is sufficient enough for a fairly arithmetic unit speed in WSNs. Similarly, HISPREC also has an area of $(6n + 2)A_{FA}$ with low cost hardware requirements and power usage and also a delay of $(9n + 2)t_{FA}$ that provides relatively low conversion delay and high performance for the WSNs in terms of energy usage and improved reliability when

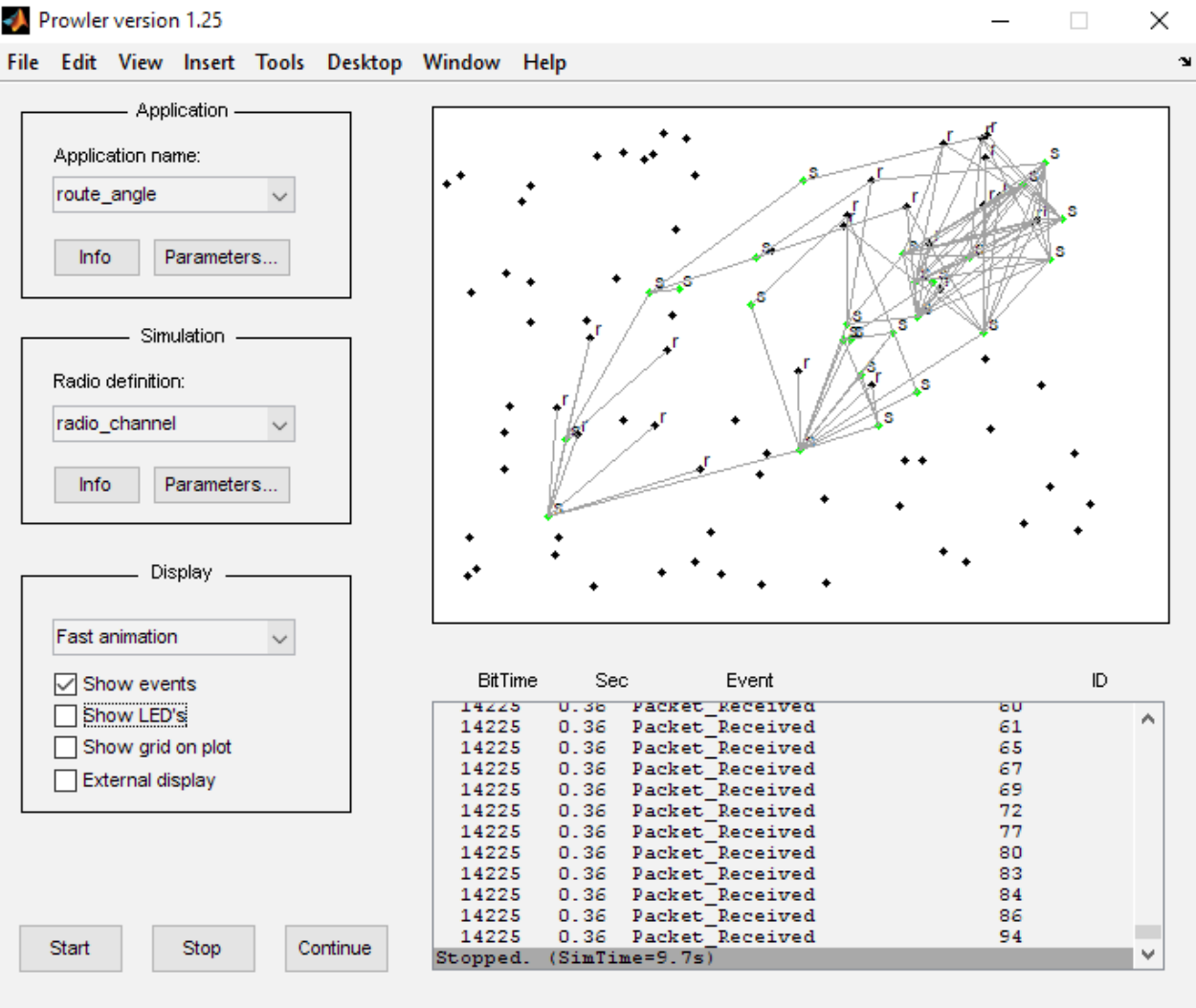


Figure 5: Sensor nodes deployed in sensor field

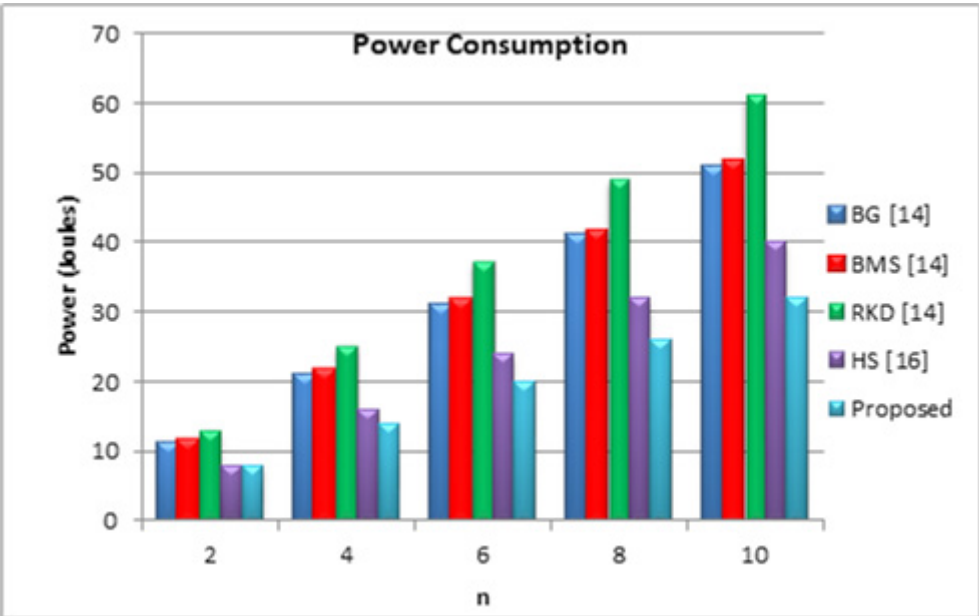


Figure 6: Power consumption and network life time

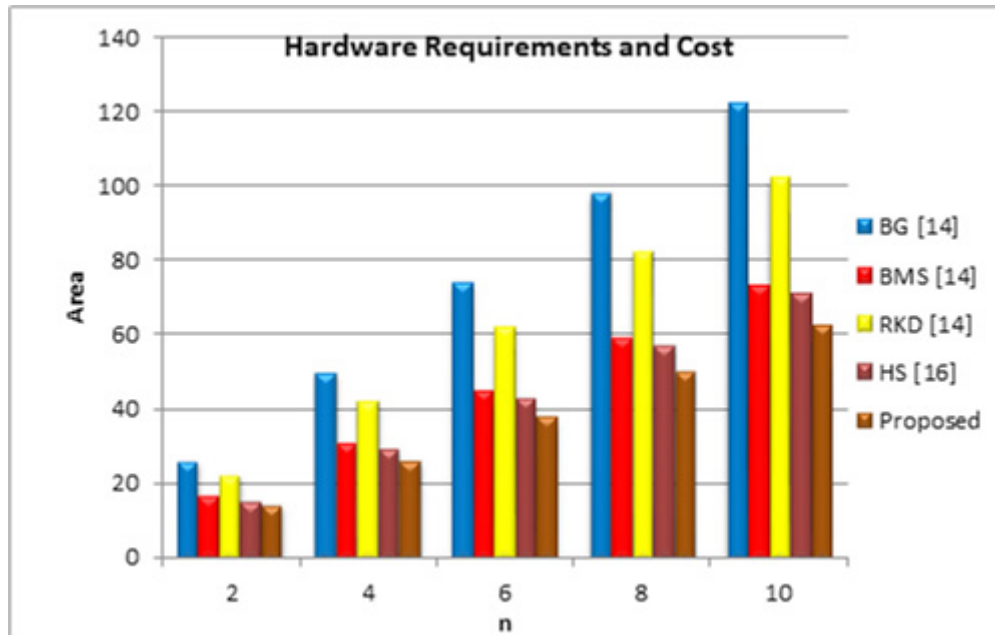


Figure 7: Hardware requirements and cost

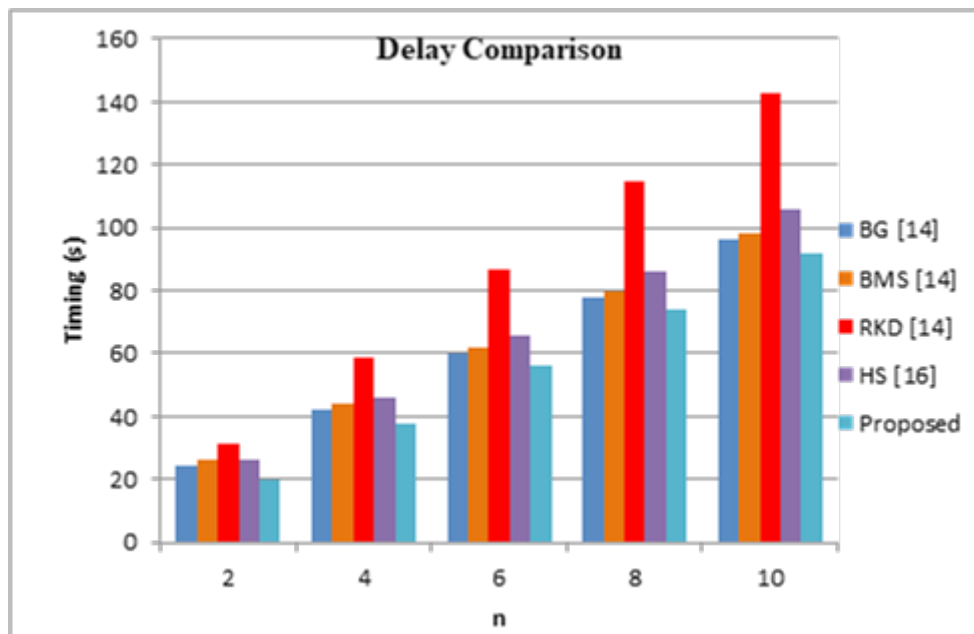


Figure 8: Conversion delay comparison

compared with other reverse converters. Finally, as shown in Figure 6, HISPREC consumes considerably about 47.5% lesser amount of energy when compared with other converters investigated. Similarly, Figure 7 indicated that HISPREC has around 49.18% less hardware requirements and cost less than other examined reverse converters. Lastly, Figure 8 clearly shows that the HISPREC produces about 35.66% lesser conversion delay as compared to other studied reverse converters.

6. Conclusion

Wireless Sensor Network consisting of spatially distributed autonomous devices using sensors to monitor physical or environmental conditions such as sound, pressure, temperature, and so on, cooperatively pass their data through the network to a sink. An efficient deployment of WSN depends on successful implementation of reliability framework. High speed reverse converter (HISPREC) for the moduli set $\{2^{n+1}-1,$

$2^n, 2^{n-1}$ is proposed. The reverse converter was designed for the moduli set $\{2^{n+1}-1, 2^n, 2^{n-1}\}$ and implemented based on MRC. HISPREC outperforms existing reverse converters in terms of speed, vitality utilisation and conversion delay in real-time WSNs. Hence, HISPREC has supremacy in terms of hardware requirements, conversion delay and speed of operations in comparison with the other reverse converters examined.

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